

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on December 21, 2000, and the reference cited therewith.

Claims 20 and 26 are amended, and claims 27-56 are added based on subject matter present in the specification; no new matter has been added. As a result, claims 20- 56 are now pending in this application.

Objection to the Specification

The disclosure was objected to because of various informalities. These informalities have been rectified per the Examiner's suggestions.

Double Patenting Rejection

Claims 20 - 26 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 7 of U.S. Patent No. 6,156,604. A terminal disclaimer will be submitted upon an indication that all claims are otherwise allowable.

Rejections Under 35 U.S.C. § 102

In the Office Action, claims 20, 21, 23 - 26 were rejected under 35 U.S.C. § 102(b) as being anticipated by Gotou (U.S. Patent No. 5,001,526).

A rejection under 35 U.S.C. § 102(b) requires that the reference cited disclose every claim limitation in the claim(s) rejected *as arranged in the claim(s)*.

Gotou appears to disclose a memory device having a plurality of semiconductor pillars each having, in order outward from the substrate, an insulating layer of silicon dioxide, a first N-type (N+) high-impurity concentration layer, a P-type (P-) low-impurity concentration layer, a P-type channel layer, and a second N+ layer. Gotou, Col. 3, line 64 to Col. 4, line 3.

Applicant's' claimed invention, as set forth in amended claim 20, includes a transistor that has, *in order*, a first source/drain region, a unitary body region, and a second source/drain region. Also, Applicant's claimed invention as set forth in claim 25, includes a first conductivity

type first source/drain region layer on a substrate, a second conductivity type body region layer on the first source/drain region layer, and a first conductivity type second source/drain region layer on the body region layer.

Comparison of Gotou and Applicant's claimed invention reveals that Gotou does not disclose the layers in Applicants' claimed invention in the order set forth in claims 20 and 25. In particular, Gotou discloses a body region that is made up of two different types of material, namely a P-type channel layer with an impurity concentration of $1.0 \times 10^{16} \text{ cm}^{-3}$, and a P⁻-type substrate layer with an impurity concentration of $1.0 \times 10^{15} \text{ cm}^{-3}$. In contrast, Applicant's claimed invention has a unitary body region, i.e., a body region formed from a single material. This provides for a more uniform, streamlined fabrication process.

Accordingly, application of Gotou as a 102(b) reference to claims 20 and 25 is inappropriate. Further, application of Gotou as a 102(b) reference to claims 21-24 depending from claim 20 and to claim 26 depending from claim 25 is inappropriate.

In light of the above, Applicants' respectfully traverse the rejection of claims 20, 21 and 23-26, and believe these claims to be patentable and thus in condition for allowance.

Rejections Under 35 U.S.C. § 103

In the Office Action, claim 22 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gotou (U.S. Patent No. 5,001,526) in view of Kimura (U.S. Patent No. 5,177,576). Examiner has applied Gotou to claim 22 in the manner applied to claims 20, 21, 23-26 in connection with the rejection of the latter claims under 35 U.S.C. § 102(b). For the reasons as set forth above, Applicant submits that the rejection of claim 22 under 35 U.S.C. § 103(a) is traversed by virtue of the amendment to claim 20 from which it depends, the amendment made in connection with the rejection of claim 20 under 35 U.S.C. § 102(a). Accordingly, Applicant believes claim 22 to be patentable and thus in condition for allowance.

AMENDMENT AND RESPONSE

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Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

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CONCLUSION

Claims 20 and 26 are amended herein. Claims 27-56 are added hereby. Claims 20-56 are now pending.

Applicant believes the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. Please charge any fees deemed necessary to Deposit Account 19-0743. The Examiner is invited to telephone the below-signed attorney at 612-373-6913 to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 24th day of April, 2001.

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